THREE CHANNEL I.F. MULTIPLEXERS

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ABSTRACT

This paper describes the first integration of multiple I.F. functions into highly integrated GaAs MMICs for electronic warfare applications. The I.F. functions include amplifiers, switches, and attenuators combined into three channel I.F. multiplexers. The multiplexers provide three channel selectivity and variable gain in each channel for application in wide bandwidth, high dynamic range electronic warfare receivers.

SUMMARY

The I.F. section of a typical microwave multi-channel receiver is large and expensive, due to the large quantity of individually tested packaged components. These individual packages consist of gain blocks, attenuators, switches, and filters. Characteristics such as VSWR, and channel to channel amplitude and phase match may be compromised by package parasitics and interactions between packages. Improvements in performance margin and repeatability, anticipated by implementing GaAs MMICs rather than GaAs or silicon discrete components, may not be realized because of the variables introduced by each package. Fully operational multi-function integrated components have been previously described [1] [2]; however, for widespread applicability of such components, testing and packaging complexity must be minimized.

In this paper we describe the development and performance of a set of I.F. MMIC multiplexers which combine previously evaluated voltage variable attenuators, amplifiers, and SP3T switches. Several considerations are described which reduce I/O connections, simplify package requirements, and reduce overall testing complexity. These considerations have resulted in a set of highly integrated components which are expected to significantly reduce testing and packaging cost and reduce I.F. section complexity.

MULTIPLEXER DESCRIPTION

Several three channel multiplexer chips have been fabricated and tested, one of which is shown in Figure 1. As shown in Figure 2a and 2b, each MMIC is composed of a combination of two or more amplifiers and attenuators, and one SP3T switch. In each implementation, the pre-filter multiplexer provides variable attenuation in each of the three signal paths. The two post-filter multiplexers provide unique arrangements of gain. The implementation shown in Figure 2a provides nominally 20 dB of gain on each of the three channels, and as much as 40 dB of gain on channel 1. The implementation shown in Figure 2b provides as much as 20 dB in channels 1 and 2. In both applications the multiplexers provide variable gain on each of the three channels.

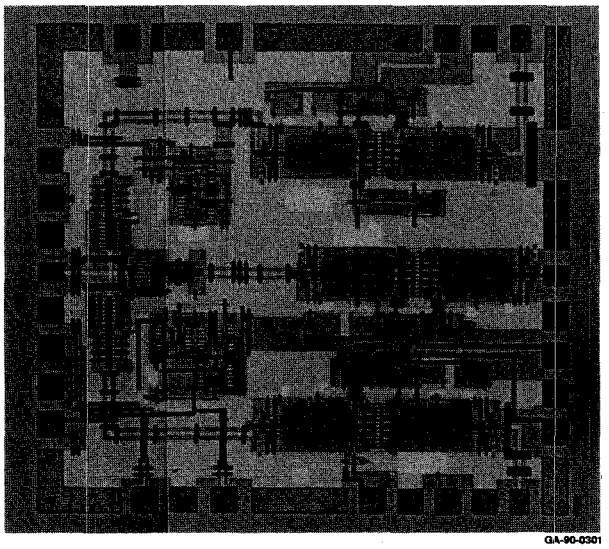

Figure 1. MMIC Pre-Filter I.F. Multiplexer. Size = 5.7mm²

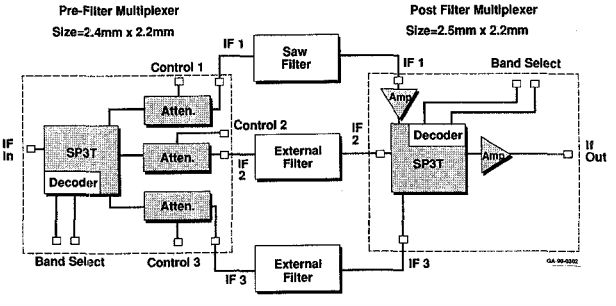

Figure 2a. Implementation of Multiplexer with Design 1 Post-Filter Multiplexer

The functions which comprise the multiplexers were individually fabricated and tested. Each component uses a coplanar waveguide topology so as not to require via holes. This approach also accommodates wafer level RF test. Air bridge inductors and MIM capacitors are implemented for impedance matching and bias networks. Implanted GaAs resistors and FET current sources are used for biasing the

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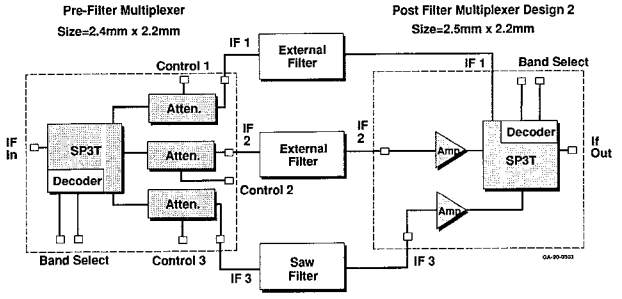


Figure 2b. Implementation of Multiplexer with Design 2 Post-Filter Multiplexer

amplifiers. The amplifiers used in the multiplexers have +15 dBm output power at the 1dB compression point. The attenuators and the switches demonstrate 15 dBm and 20 dBm, respectively, of output power at the 1 dB compression point, in order to minimize distortion.

These multiplexers are ideally suited for broadband EW receivers. A three channel Ford Aerospace EW receiver has been selected as the insertion candidate. This receiver has three bands of I.F. resolution. Presently, the receiver implements individually packaged functions. Two switches are required to select the appropriate filter and one or more amplifiers are required to compensate for filter loss in each channel. This implementation requires at least six packaged components (not including filters). Fixed attenuator pads are used to balance the gain through each channel. The same function is performed in MMIC by two multiplexers which channel the I.F. signal to the appropriate filter. The ability to adjust gain separately through each channel will accommodate varied filter types (lumped element, printed thin film, and SAW) and will allow gain equalization. This is particularly useful for developmental work were the loss through filters may not be known, or where channel to channel matched gain is a key system driver.

CONSIDERATIONS FOR HIGH INTEGRATION

The circuits selected for use in the multiplexer were each individually fabricated and tested prior to subsequent integration. The components were then selected because of their repeatability and high performance margin in the band of interest (0.2 to 2 GHz) [3]. The total gate periphery for the attenuator is 6.7 mm with a total of 13 FETs. The total gate periphery for the switch is 5.9 mm with a total of 57 active elements. The gate periphery of the amplifier is 3.3 mm with a total of 4 FETs.

The high level of integration also requires good uniformity across several square millimeters of active semiconductor area. Early attempts to obtain highly integrated components with areas greater than 3mm^2 were constrained by variable process parameters or defects which caused at least one function of a multi-function chip to fail or perform below standards. A multiple level passivation, including passivation of the gate with polyimide, prior to subsequent metal deposition, substantially reduced this problem. To quantize the yield, ten of each type of multiplexer from a single wafer were packaged (only ten of each type were available due to the large number of other components on the wafer). Of the ten multiplexers packaged from a single wafer, 8 of these were fully functional. The two failures were attributed to damage during the packaging procedure.

In each design, the chip size was reduced in order to increase circuit throughput. Highly integrated circuits which perform many functions will be size-limited by the number of I/O pads. Each I/O pad is required to be 100 um^2, with a 150 um pitch to adjacent ground pads, in order to enable wafer level probing of the multiplexer and to allow reliable bonding. Initial integration attempts identified the key problems associated with this size limitation. Firstly, the large number of functions initially indicated a large number of I/O pads, and consequently an undesirably large chip. Secondly, the multiplexer with a large number of I/O pads would have been impossible to wafer level probe, and very difficult to package and test. Finally, the low cost package which was intended for system insertion would not accommodate the number of I/O connections initially proposed.

In order to overcome these problems and reduce the number of I/O pads several features were designed into the subcomponents to reduce I/O requirements. The SP3T switch implements a decoder which requires two TTL compatible inputs to select one of three channels, and a positive and negative voltage supply. Without this decoder, the three channel switch would require six control voltage I/O connections. The attenuator was also designed to minimize I/Os and reduce control signal complexity. Originally, the attenuator required two control voltages (one on the shunt FETs and one on the series FETs) to achieve the desired attenuation. The attenuator voltage control was simplified by waveform shaping circuitry which creates a differential voltage for control of the series and shunt attenuator FETs from a single control voltage. The waveform shaping circuitry is designed to maintain a 2:1 VSWR on the input of the attenuator through all attenuation states. Although the waveform shaping circuitry requires positive and negative supply voltages, no additional I/Os are required on the multiplexer for these supplies, as these already exist on the MMIC. Since there are three attenuators on a chip, three additional I/Os were eliminated per chip.

Even with the judicious elimination of bond pads, the minimum size of the multiplexer is limited by several factors which are characteristic of highly integrated circuits. Firstly, large DC de-coupling capacitors (>25pF) are used on each of the bias nodes of the amplifiers to avoid bias coupled effects. Secondly, fairly large DC blocking capacitors (12pF) are used to maintain 50 ohm impedance between the individual components on the MMIC substrate. Finally, the active region of the amplifiers on the MMIC are separated by more than 0.6 millimeter to enhance power dissipation (as much as 0.9 W per amplifier) in the 10 mil thick substrate. The optimal size for each multiplexer was determined to be approximately 5.7 mm^2.

The multiplexer in the package is shown in Figure 3. The package selected for these designs was a very low cost (approximately $7.00) flatpack. To minimize degradation of circuit performance due to the package the circuits were designed to absorb a small amount of bond wire inductance in the input and output matching networks. Additionally, the multiplexers are only slightly smaller than the internal cavity of the package, thus the bond wire inductance, from MMIC to package, was minimized. Only slight degradation in chip performance was observed when packaged.

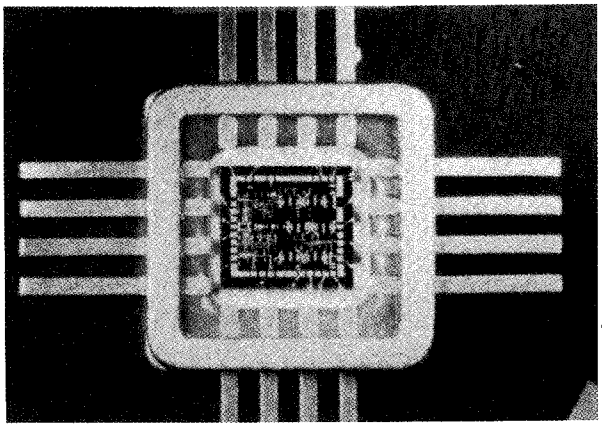


Figure 3. Multiplexer in Low Cost Commercial Flatpack

MULTIPLEXER PERFORMANCE

The multiplexers were tested in a setup replicating the final system brassboard. The variable attenuation (measured at the wafer level) through one channel of the pre-filter multiplexer is shown in Figure 4. The channel is selected by two TTL compatible control signals. The attenuation is adjusted independently in each channel by a single control voltage. Each of the three channels operate identically. The pre-filter multiplexer does not contain any gain blocks and is used only to multiplex the I.F. signal and provide 30 dB of variable attenuation on each of the three channels. The input and output VSWR is better than 2:1 in all of the attenuation states.

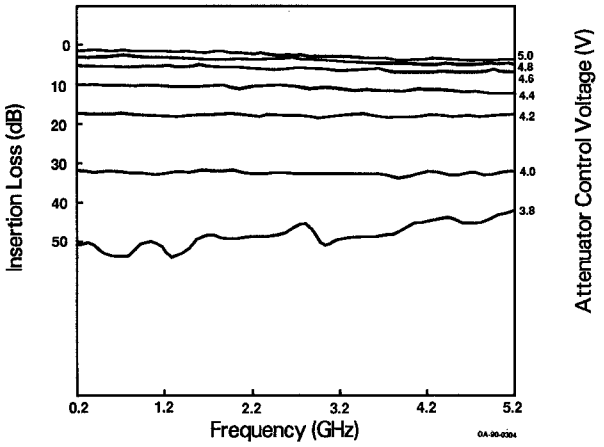
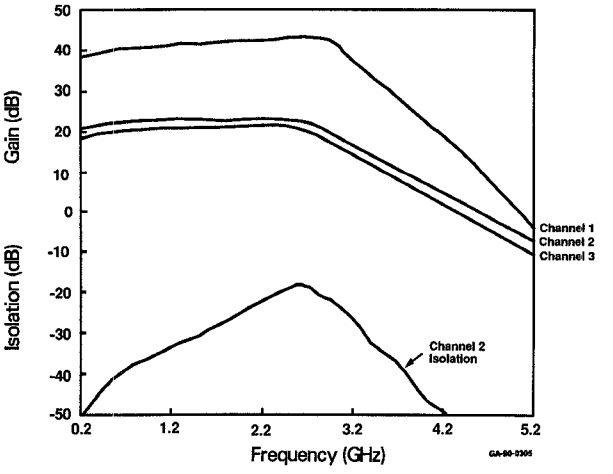


Figure 4. Flat, Voltage Controlled Attenuation Levels are Obtained over a Wide Frequency Range

The wafer level performance of the two post filter multiplexers is shown in Figures 5 and 6. These multiplexers are comprised of unique configurations of amplifiers to provide 0, 20 dB or 40 dB of gain. The channel is selected by two TTL compatible control signals. Channel to channel isolation is 30 dB or more. Input and output VSWR is better than 2:1 on all channels.

The 1 dB bandwidth of the multiplexers is reduced from 2.7 GHz to 2.0 GHz when mounted in the package. No



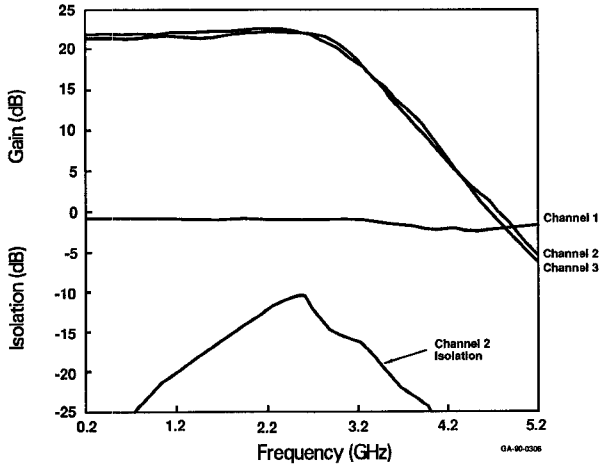


Figure 5 and 6. Performance of Two Versions of the Post-Filter Multiplexers Show Flat Gain and High Isolation Over a Wide Frequency Range

degradation in isolation or VSWR is attributable to the package below 2.0 GHz.

CONCLUSION

Three I.F. multiplexer designs have been fabricated and tested. The multiplexers provide variable gain in each of three channels selected by TTL compatible control lines. The multiplexers demonstrate very high integration multi-functionality. An important aspect of this development was the highly repeatable nature of the individual circuit designs selected and the wafer process uniformity. However, process uniformity alone does not ensure that the high integration component can be successfully tested and packaged. Implementation of the highly integrated circuit requires minimization of bond pad connections to enhance testability. Over-all low cost is achieved by using a low cost commercial package. Circuit design philosophy must anticipate package deficiencies and account for parasitic inductance. Significant reduction in

packaging cost and testing cost is anticipated with these multiplexers, relative to the cost of packaging and testing individual circuit functions.

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